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A Hypothetical Approach of Designing Novel Reversible Combinational Logic

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ABSTRACT : *Reversible logic attained major height in the contemporary research interest by leaps and bounds due to its low power consumption like design specs. The reversible logic has commencing future in CMOS design, bioinformatics, optical information processing, cryptography and nano electronic circuits. On the other hand logic circuits for digital system perform a specific information processing operation. It is designed by a set of Boolean function. This manuscript presents a novel design idea namely JSM reversible logic gate & simultaneously depict the prototype of some combinational logic circuit architecture (i.e. half adder, half-sub-tractor & 1 bit comparator) by using the reversible proposed JSM gate.*

Keywords-*Combinational Logic, Constant Input, Garbage Output, Quantum Cost, Reversible Logic Gates.*

I. INTRODUCTION

Consumer electronics is not a luxury but it is indispensible in today's human life. Since long, engineer's attempted several metaphors to articulate high speed low power consuming & low power dissipating consumables electronics. In this regard reversible logic can be viewed as an added advantage. But still the limiting factor of electronics equipment's is power dissipation. According to Moore's law the number of transistor that can be cramped in integrated circuits should double in every 18 months. As more and more transistors are added in integrated circuits, it produces enormous amount of heat. Scientist & Engineers strive hard to make this power dissipation low [Landauer & Bennett] [1], [2]. Launder invented an irreversible logic circuit. Each bit of information in this circuit generates KT ln2 Joules of heat energy. Bennett proved that the KT ln2 amount of energy dissipation would not occur if the computation can be done by reversible way. Thus, Reversible logic is best suited for quantum computing & nano technology based low power architectural synthesis. This manuscript presents a hypothetical modeling of the reversible logic based design.

II. THE IDEOLOGY OF REVERSIBLE LOGIC GATES

The reversible logic operation processes information by merely dissipating very less heat. The demand of reversible circuit in high speed low power consuming device is increasing day by day. Besides, reversible logic [3] has one to one mapping. Due to one to one mapping the input vector can be determine by output vector. The computational aspect of reversible logic is that

Input(s) + constant input(s) = output(s) + garbage output(s).

Few distinctive features about reversible logic gate is that

1) The number of output(s) = the number of input(s).
2) Fan out is not allowed.
3) The garbage should be less. But garbage output is unavoidable to get the reversibility.

III. FEYNMAN / CNOT GATE (FG):

Fig 1 depicts the block diagram of 2*2 Feynman gate [4]. It is also called as Controlled NOT. The inputs are A and B and outputs are P=A, Q= A⊕B. Its Quantum cost is 1. Feynman gate can be used as copier or compliment.

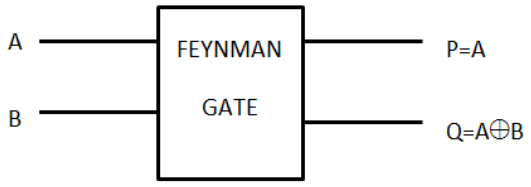

Fig.1- Feynman Gate

IV. PROPOSED REVERSIBLE LOGIC GATE

In this paper we proposed a new 3*3 reversible logic gates called JSM gate. This reversible gate is named after first letter of the authors' name. The modus operandi of the proposed JSM gate is depicted in the fig.-2 in the following. The proposed JSM gate consists of 3 inputs i.e. A, B &C whereas the outputs are P=A, Q=(A+B)⊕C, R= $\bar{A}C \oplus AB$

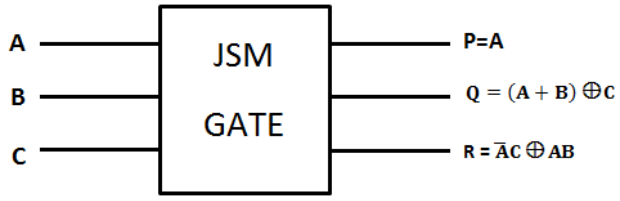

Fig-2 JSM Gate

The truth table of the proposed JSM gate is derived in the following

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1

The authors here for further analytical study relied upon the soft computation. Initially the JSM gate was simulated by Xilinx ISE 14.5[5], [6] and the simulation result is given is below.

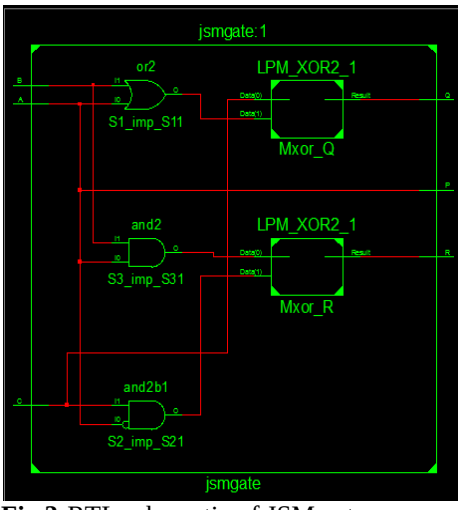

Fig.3-RTL schematic of JSM gate

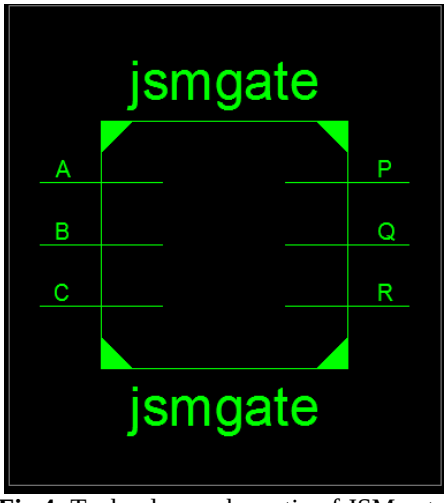

Fig.4- Technology schematic of JSM gate

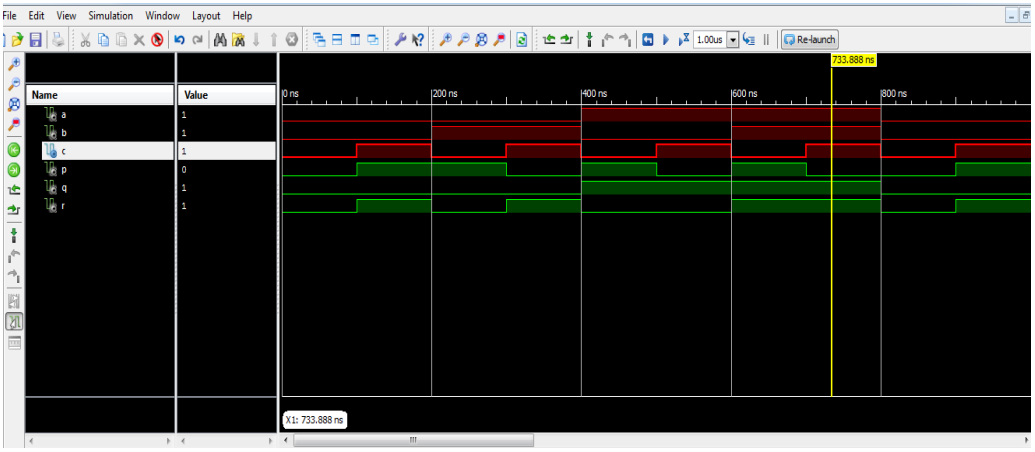

Fig.5-Simulation result of JSM gate in Xilinx 14.5. The red and green colored signals are accordingly inputs and outputs signal.

V. COMBINATIONAL LOGIC CIRCUIT USING JSM GATE

To investigate the merits of JSM gate the authors designed half adder, half sub-tractor and 1 bit magnitude comparator using this JSM gate [4], [5].

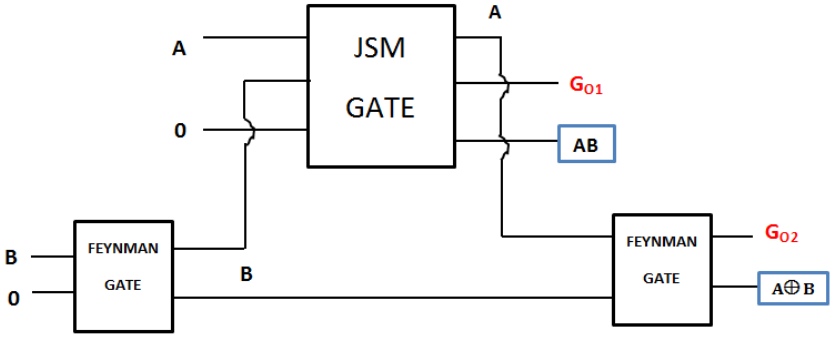

Fig.6 half adder

Fig. 6 shows the half adder. 1 JSM gate and 2 Feynman gate is used to design half adder. There are two inputs with two constant inputs (0, 0).the outputs (A—B, AB) are shown in blocks. G_{01}, G_{02} are the two garbage outputs.

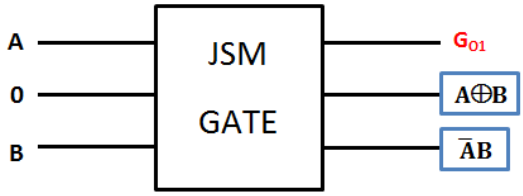

Fig.7 half sub-tractor

Fig.7 shows the half sub-tractor. The half sub-tractor is designed using one JSM gate. There are two inputs (A, B) and one constant input(0) . The outputs are (A—B, $\bar{A}B$). G_{01} is the garbage output [7].

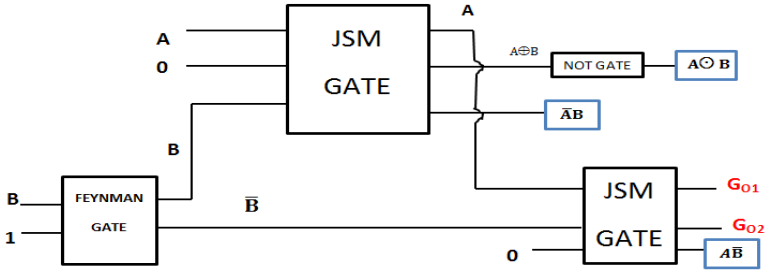

Fig8. 1 bit magnitude comparator

Fig8. Shows 1 bit magnitude comparator. Two JSM gate, one Feynman gate and one not gate is used to design it. There are two inputs (A, B) and three constant inputs (0,0,1). Outputs (A⍱B, $\bar{A}$B, A$\bar{B}$) are shown in blocks. G_{01}, G_{02} are the two garbage outputs [8].

VI. CONCLUSION

The proposed JSM gate is exclusively noteworthy. Although it is quite simplistic & straight forward in nature but it is pivotal in designing next generation combinational circuit. The modeling is in good agreement with the contemporary CMOS irreversible logic. The quantum cost lies in proximity to the satisfactory level. Thus the hypothetical approach is anticipated to be unanimously accepted in future combinational logic designing.

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